

Low-Cost Embedded NVM for Power Management Designs

Yakov Roizin, Evgeny Pikhay, Amos Fenigstein, Avi Strum

Tower Semiconductor Ltd., P.O.Box.619, Migdal HaEmek 32105, Israel

In this paper we present two unique NVM solutions which can close two significant gaps in the embedded memory IC world. Today's designers have a large choice of embedded non-volatile memories (NVM) verified in different production technologies. These memories can be divided into three groups:

- (i) true MTP (multiple-time-programmable) having densities up to several tens of Mbit and endurance of >100 K program/erase cycles [1,2]
- (ii) OTPs (one-time-programmable) fabricated without additional masks, enabling NVM modules up to 1 Mbit [3];
- (iii) small size (up to several tens Kbit) MTP or FTP (few-times-programmable) without mask adders [4,5].

True MTP usually requires over 10 additional masks to the core CMOS. OTP modules can not be used efficiently for memory sizes larger than 1 Mbit due to reliability limitations, and also are limited in field applications. The no added mask MTP solutions are area consuming and usually limited to no more than a few tens of Kbits. Cost-efficient MTP solutions for middle-sized (<1Mbit) and large (>1Mbit) embedded memories are not available.

In the design of power management (PM) ICs, similar to other application fields, embedded NVM at no additional cost is one of the main value-added differentiators. Both small-size NVM for trimming of analog parameters, feature selection, address storage, etc., and larger NVM modules for code storage, system configuration and security applications are challenging. Nevertheless, to find a low-cost embedded NVM for a typical 0.18/0.13um PM process flow (technology nodes compromising production costs and availability of cutting-edge IP libraries [4]) is much more difficult than for standard logic applications. Compared with standard logics, PM chips are typically designed for a more robust 5V only or 5V/1.8V operation, even if larger silicon area is required. Thicker GOX in the 5V designs implies high operation voltages, thus requiring area consuming charge pumps, complicating field programming and introducing additional reliability limitations in the scaled down core CMOS. The known MTP NVM solutions

suitable for PM IC have very large cell areas, thus adding significant die area even for small size embedded modules. OTP NVM solutions do not allow field upgrades and do not support 5V I/O voltage typically used in power management ICs.

In this paper we report on two novel types of low-cost memories (Y-Flash and S-Flash) suitable for PM, both having record cell sizes in their application fields. The memories are highly scalable and can be embedded into typical CMOS process flows (specifically, but not limited to 0.18um and below) without additional masks or with up to two additional non-critical masks (for memory performance enhancement).

Y-Flash is targeted for 1Bit to 1Mbit memory modules. It has an original “asymmetric” two-terminal cell design with only $\sim 2 \text{ um}^2/\text{Bit}$, and allows more than 100,000 program/erase cycles. Y-Flash is supposed to close the mentioned “low-cost middle-sized MTP” gap in the NVM market. Fig.1 shows the Y-Flash operating principle and a layout of a typical Y-Flash cell. An asymmetric transistor having a Poly

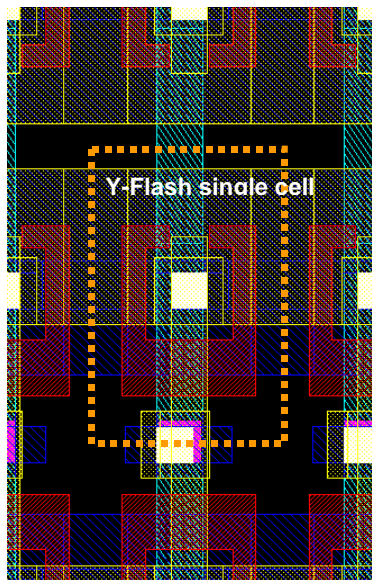
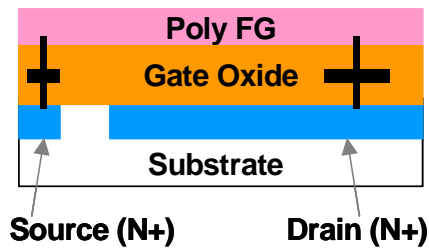


Fig.1 Cell design and layout of Y-Flash

floating gate (FG) is formed by a standard CMOS process flow. The FG has a portion disposed over the channel region and an additional portion extending into an enlarged drain diffusion area away from the channel region. The gate-to-drain capacitance is thus significantly higher than the gate-to-source capacitance. The width of the FG extension portion is minimized, enabling LDD implant merging under the floating gate extension. The HV LDD implant in the NVM transistor is substituted by other implants from the core CMOS process. Programming is performed by applying a positive programming voltage to the drain region and connecting the source region to ground, thereby causing channel hot electron (CHE) injection from the drain region into the FG. In the low-power flavor, the memory cell is placed into an insulated p-well to allow programming with more efficient CHISEL (secondary electrons) mechanism that assumes substrate bias. Erasing the floating gate involves connecting the drain diffusion to ground and applying the positive voltage to the source, thereby causing band-to-band tunneling (BBT) generation of holes and their injection into the FG. There is no need for a select transistor in the Y-Flash designs. This is illustrated in Fig.2 where a simplified Y-Flash

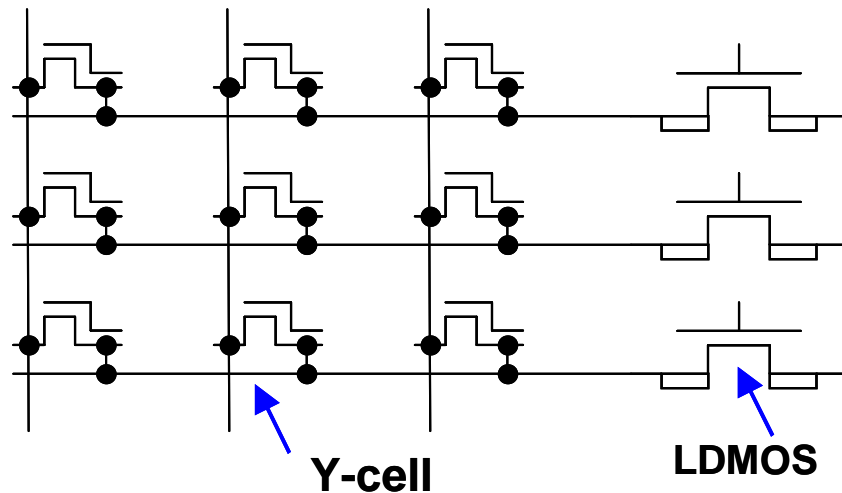


Fig.2 Y-Flash array

cross-wise memory array is shown. The row and column select circuitry is built using LDMOS transistors which are legal devices in the same core CMOS process flow (no additional masks) or by cascading solutions. Reliability studies confirm feasibility of over several hundred thousand Y-Flash program/erase cycles. A very small cell area (compared with competing single Poly FG) allows MTP modules significantly smaller

than in typical MTP designs (which are in the range of $10 \mu\text{m}^2$, 5x larger than the Y-flash cell). Accordingly, asymmetric Y-Flash are ideal for incorporating into low cost CMOS integrated circuits requiring several Kbits up to 1Mbit of high endurance memory.

In many high density (>1Mbit) embedded applications there is no need for true MTP. A typical example is a microcontroller code which is not changed too many times. In such cases, it would be favorable to replace the designs currently using true MTP large volume embedded flash with low cost solution. Though having a record memory cell size among single Poly FG memories, Y-Flash becomes too area consuming for modules exceeding 1Mbit. Instead, S-Flash is targeted for the use in applications requiring cost-effective high density (1Mb-32Mb) FTP embedded memories. S-Flash employs Tower patented spacer trapping principle[6] and has an extremely small cell size ($<0.2\mu\text{m}^2/\text{Bit}$, close to the well known Tower's *microFlash*[®] and Saifun's NROM[®][2]). The principle of S-Flash is illustrated in Fig. 3.

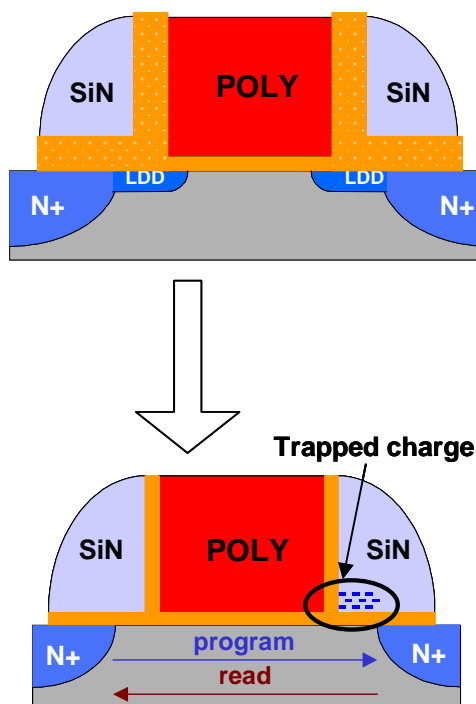


Fig.3. S-Flash principle

In a standard CMOS manufacturing process, the nitride of spacers is deposited on a thick ($\sim 200\text{\AA}$) CVD oxide. Decreasing the bottom oxide (BOX) and sidewall oxide

thickness, skipping of LDD extensions and performing special drain engineering to enhance lateral fields in the drain region, facilitates trapping of electrons in the nitride. A standard n-channel MOS transistor is thus converted into a non-volatile memory cell. The trapped in the spacer electron charge is monitored in a reverse read-out scheme [2]. Two bits of information (in the spacers from both sides of the gate) are stored in a single memory transistor, similar to NROM memories. The cell can be erased by hot holes, generated by the BBT mechanism like in NROM and Y-Flash. Program/erase characteristics of a typical S-Flash cell are presented in Fig.4. The results demonstrate large memory windows and small programming times necessary for operation of large NVM arrays.

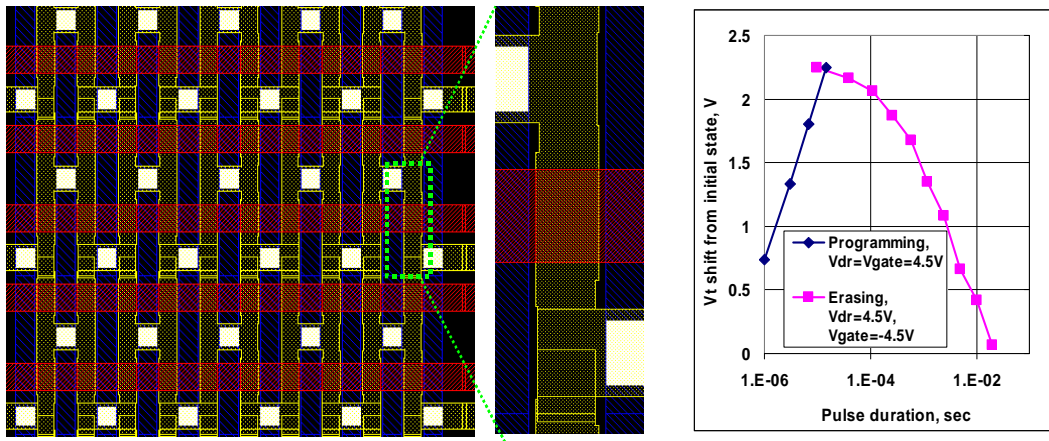


Fig.4 S-Flash. Program/erase kinetics and H-array design

The S-Flash memory was verified on Si using 2MBit Array-TEG. Area saving H-array geometry [6] is employed in the existing designs (Fig.4). The S-Flash memory allowed reliable operation up to ~ 100 program/erase cycles. Programming and erase with voltages below $|5|V$, excluded the need of special high voltage periphery circuitry. No disturb issues different from those known for NROM memories were revealed in the studied range of cycles and employed voltages. The high volume S-Flash memory is embedded into the standard CMOS process with only two non-critical masks added and minimum additional process operations.

In summary, two original Tower NVM technologies allow the design of low-cost memory modules covering all practically necessary sizes of NVM in embedded PM applications. A record for single Poly MTP memory cell size and simple array design

with no mask adders makes, in some cases, the single Poly Y-Flash as effective as the true MTP Flash, with no additional cost, typically associated with a true MTP solution. S-Flash featuring one of the smallest in the industry cell size, is the cheapest FTP large volume memory solution not requiring special periphery devices and having outstanding retention performance.

References

1. <http://www.sst.com/technology/superflash/701.xhtml>
2. B. Eitan, et.al IEEE Electron Device Letters, v.21 , 543, 2000.
3. <http://www.eetimes.com/showArticle.jhtml?articleID=209900470>
4. <http://www.powermanagementdesignline.com/howto/showArticle.jhtml?articleID=187201992>
5. B. Wang and Y. Ma, NVSMW-ICMTD08, 2008 pp.22-26
6. Y.Roizin and A.Fenigstein, US Patent 7,227,234, 2007

Yakov Roizin, Senior Staff Member and NVM R&D Manager at Tower, has more than 30 years of semiconductor device development experience. He received his Prof.,Dr.Sc.Hab and Ph.D. degrees from the leading Academia institutions in the former Soviet Union . In the past 12 years he has been working on the development of non-volatile memories. He is the author of more than 120 research papers and 30 patents in the field of semiconductor electronics.



Evgeny Pikhay, Senior Device Engineer at Tower, graduated from the Technion-Israel Institute of Technology and has 7 years of experience in embedded NVM development. He is an author of papers and patents on advanced memory solutions.

Amos Fenigstein, R&D Director at Tower, has over than 15 years of semiconductor-industry experience in engineering and management, Amos received his B.Sc, M.Sc. and D.Sc. degrees from the Technion-Israel Institute of Technology. Before joining Tower in 2001, he was with Intel Corporation, managing a failure analysis team. His current research activities are in the field of embedded applications, including non-volatile memories, embedded power devices and CMOS image sensors.

Avi Strum, Vice President and General Manger of Tower Specialty Product Line, received his B.Sc., and Ph.D degrees from the Technion-Israel Institute of Technology and has over than20 years of semiconductor industry experience. He is responsible for engineering, R&D activities and product marketing in the fields of NVM, Power Management, core CMOS and CMOS image sensors. Prior to joining Tower he directed R&D activities and held strategic management positions at several semiconductor companies including Intel Corporation. Avi's email address is: avist@towersemi.com